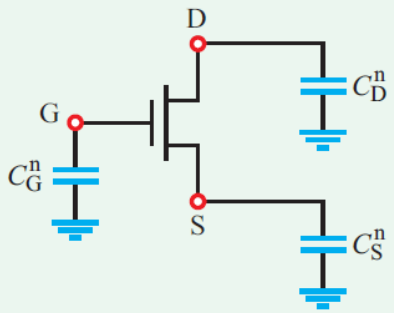
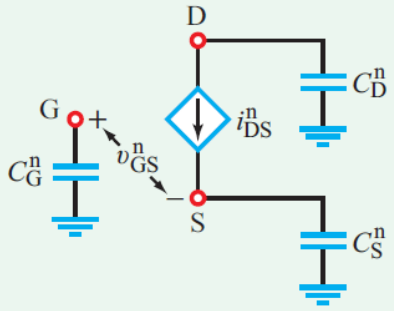
Concept Question 5-26: What is the rationale for adding parasitic capacitances to nodes G, D, and S in Fig. 5-48?



(a) NMOS



(b) Equivalent circuit

Figure 5-48: n-channel MOSFET (NMOS): (a) circuit symbol with added parasitic capacitances and (b) equivalent circuit. [In a PMOS, parasitic capacitances C_D^p and C_S^p should be shown connected to V_{DD} instead of to ground.]

These capacitances model charge storage phenomena that result from both transistor physics and metal interconnects running near the transistors. They allows us to model time transients of voltages and currents as well as energy and power constraints.